ABSTRACT OF THE DISCLOSURE

Methods and systems for generating and synchronizing multiple clocks are disclosed herein that have extremely low skew across multiple channels and latency that is both minimal and well-defined. A phase-locked loop circuit generates a plurality of clock signals to synchronize channel circuits that receive core data streams. The channel circuits convert the core data streams into serial data streams. The phase-locked loop circuit or another phase-locked loop circuit generates a core clock signal for the registered transfer of the core data streams to the channel circuits. One or more of the plurality of clock signals may be distributed to the channel circuits by a register-to-register transfer.